→ Output2 ◆ Output1 16 Multiplexer 3 delay line: $\triangle L (\triangle au)$ Phase Adjustment Φ _<u></u>= FDM M PRIOR ART 15 Fig. 1 Input

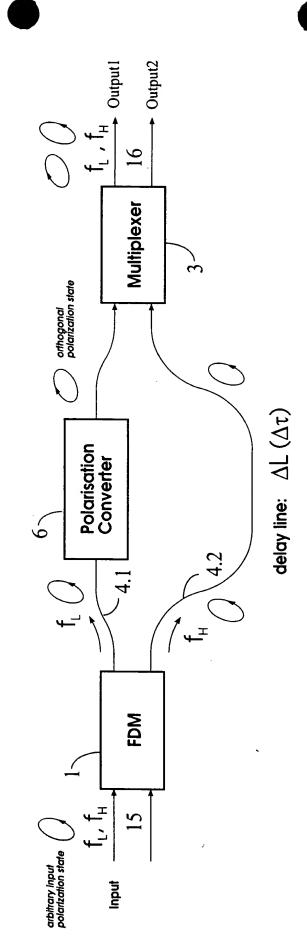
\$ Δφ. φ̈́ 5 φ. <u>.</u>

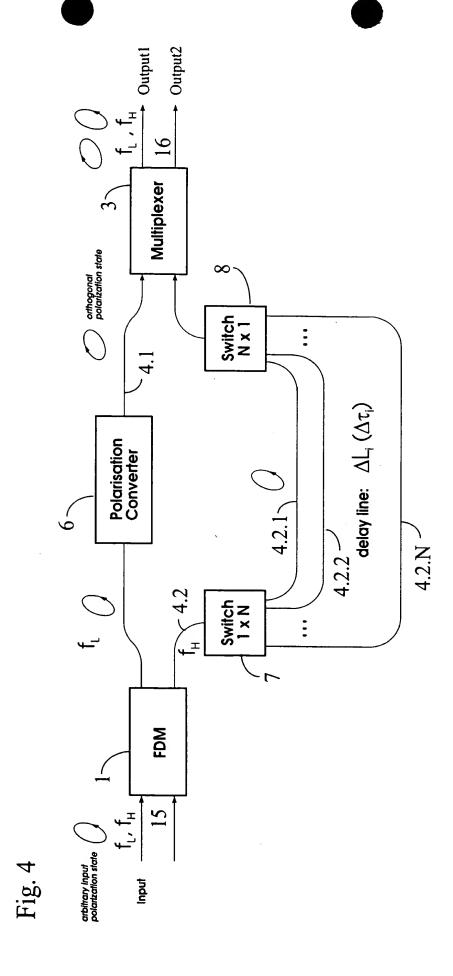
PRIOR ART

Fig. 2

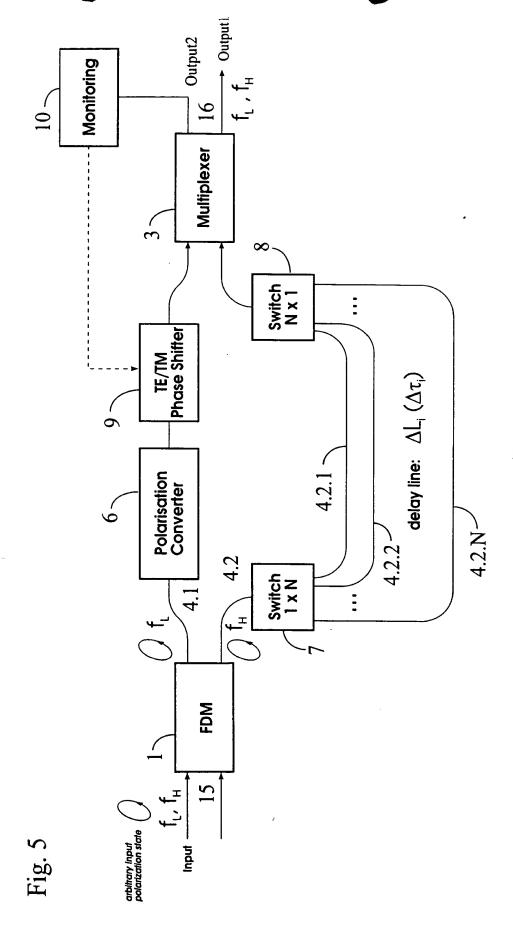
1/6

Fig. 3





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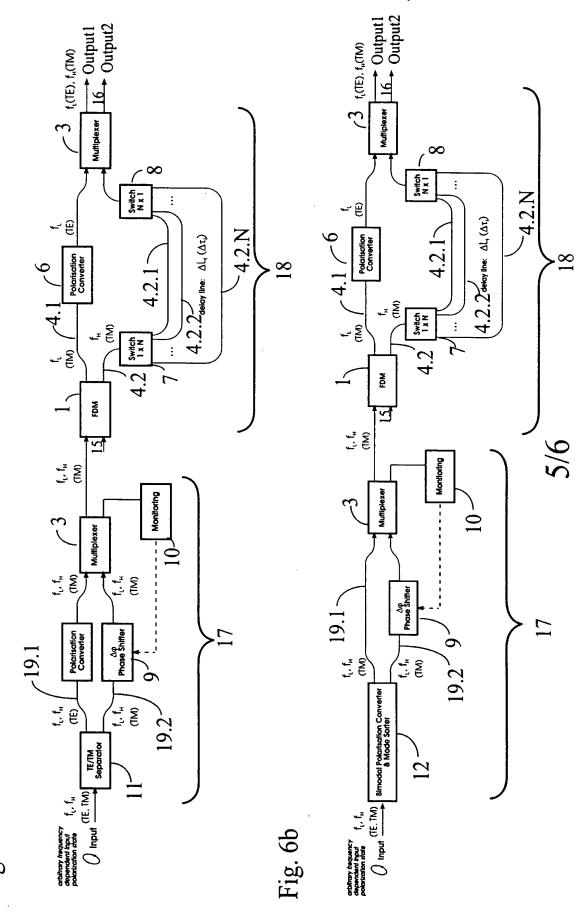


Fig. 6a

Fig. 7

